II. REMARKS

In the Final Office Action mailed on May 18, 2004, claims 1-11 were allowed. Claim 12 has been canceled. By the foregoing Preliminary Amendment, claims 13-17, 19 and 20 have been amended to clarify the claimed subject matter, without narrowing the scope of the claims. New claims 21-26 have been added. No new matter has been added. Thus, claims 1-11 and 13-26 are pending in the Application. Reconsideration of this application is respectfully requested in view of the foregoing Preliminary Amendment and the following remarks.

As a preliminary matter, Applicants acknowledge with appreciation the allowance of claims 1-11 and the indication of allowable subject matter in claims 17 and 18.

The following remarks address the merits of the Final Office Action that require response.

A. Objection to Claim 13

At paragraph 1 on page 3 of the Final Office Action mailed on May 18, 2004, the Examiner objects to claim 13 on the basis of informalities. Claim 13 has been amended to overcome the objection. No further response is necessary at this time.

B. Rejection of Claims 13-16, 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by Ohtake, *et al.*

The Examiner rejects claims 13-16, 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,088,290 to Ohtake, *et al.* Applicant respectfully

submits that claims 13-16, 19 and 20, as amended, recite subject matter that is neither disclosed nor suggested by the Ohtake, *et al.*

With regard to claim 13, the Examiner indicates that Ohtake, *et al.* discloses each and every limitation of claim 13, including a clock buffer controller "that activates said clock buffer, only when there is a change in said input signal, so that the clock buffer generates the internal clock signal and provides the internal clock signal to said input buffer [*input buffer in activate state, clock signal CLKIN2 generated; input buffer in non-activate state, clock signal CLKIN2 not generated*; col. 4, lines 35-49]." *See, e.g.,* Office Action at page 4.

Ohtake, *et al.* fails to disclose or suggest each and every limitation of amended claim 13, which is a requirement for making out a rejection under 35 U.S.C. § 102. For example, Ohtake, *et al.* fails to teach or suggest at least the limitation of a clock buffer controller "that, upon detecting a change in said input signal, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said input buffer," as claimed in amended claim 13. Ohtake, *et al.* only discloses that a power-down control circuit sets a power-down signal at a high level in order to release a power-down mode when a clock enable signal asynchronous with a clock signal is set at a high level. When the power-down mode is released, a clock controlling section activates an internal clock signal. In Ohtake, *et al.*, upon receiving the internal clock signal, a latch circuit latches an output signal of a command decoder. Furthermore, in column 4, lines 35-49, the paragraph the Examiner cites to as disclosing the "clock buffer controller" of the present invention, Ohtake, *et al.*, merely discloses two input buffer circuits, one permanently set at a non-activate state in the power-down mode, and one permanently set at an activate state in the power-down mode.

By contrast, the clock buffer controller of the present invention, "upon detecting a change in said input signal, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said input buffer," as recited in claim 13, as amended.

For at least these reasons, Applicant submits that claim 13 is allowable over the cited prior art. As claim 13 is allowable, Applicant submits that claim 14 and new claim 21, depending from allowable claim 13, are likewise allowable over the cited prior art.

Similarly to as discussed above with regard to claim 13, Applicant submits that claims 15 and 16 are allowable over the cited prior art because the cited prior art does not disclose or suggest at least the features of a clock buffer controller[s] that, "upon detecting a change in ... said input signal[s] ..., activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said plurality of input buffers," as claimed in claims 15 and 16, as amended. As claims 15 and 16 are allowable, Applicant submits that new claim 22, depending from allowable claim 15, and new claim 23, depending from allowable claim 16, are likewise allowable over the cited prior art.

With regard to claims 19 and 20, Applicant submits that claims 19 and 20 are allowable over the cited prior art because the cited prior art does not disclose or suggest at least the features of "monitoring if there is a change in said input signal[s]," and "activating said clock buffer when the change in ... said input signal[s] ... is detected, so that the clock buffer generates said internal clock signal, in synchronization with which the input signal[s] ... is fetched," as claimed in claims 19 and 20, as amended.

For at least these reasons, Applicant submits that claims 19 and 20 are allowable over the prior art.

Furthermore, with regard to new claims 24-26, Applicant submits that claims 24-26 are allowable over the cited prior art because the cited prior art does not disclose or suggest at least the features of first and second clock buffer controllers that, "upon detecting a change in ... said ... signal[s] ..., activates said ... clock buffer to generate said ... internal clock signal and to provide said ... internal clock signal to said ... input buffer[s]," as claimed in new claims 24-26.

For at least these reasons, Applicant submits that claims 24-26 are allowable over the cited prior art.

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300, referencing Attorney Docket No. 108066-00038. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing Attorney Docket No. 108066-00038.

Respectfully submitted,

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